A Very Cost Effective Printed Circuit Board Alternative to Co-Fired Ceramic and Hybrid Integrated Circuits
A system of manufacturing Printed Circuit Boards (PCBs) employing a thermally engineered metalized material layer to enable the integrated assembly of advanced electronic circuits using both surface mount (SMT) and unpackaged die components.

Provides a very low cost alternative to co-fired ceramics and hybrid MICs.

With superior thermal conductivity and ceramic matched CTE, the ECLIPS PCB allows for direct die attach and wire bonding of high power and sensitive IC components and also standard SMT assembly of all others without degradation from dissipated heat.

The result is a smaller, more reliable and producible and much more less costly system.
## PERFORMANCE COMPARISONS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Co-Fired Ceramic</th>
<th>Hybrid MIC</th>
<th>ECLIPS PCB</th>
</tr>
</thead>
<tbody>
<tr>
<td>co-location of die &amp; SMT components on single substrate</td>
<td><strong>YES</strong></td>
<td><strong>NO</strong></td>
<td><strong>YES</strong></td>
</tr>
<tr>
<td>enables high density trace routing &amp; signal interconnections</td>
<td><strong>YES</strong></td>
<td><strong>NO</strong></td>
<td><strong>YES</strong></td>
</tr>
<tr>
<td>thermal conductivity</td>
<td><strong>POOR</strong></td>
<td><strong>EXCELLENT</strong></td>
<td><strong>EXCELLENT</strong></td>
</tr>
<tr>
<td>CTE matching die attachment</td>
<td><strong>NO</strong></td>
<td><strong>YES</strong></td>
<td><strong>YES</strong></td>
</tr>
<tr>
<td>allows automated assembly</td>
<td><strong>YES</strong></td>
<td><strong>NO</strong></td>
<td><strong>YES</strong></td>
</tr>
<tr>
<td>housing material cost</td>
<td><strong>LOW</strong></td>
<td><strong>HIGH</strong></td>
<td><strong>LOW</strong></td>
</tr>
<tr>
<td>Material cost</td>
<td>$$$$$</td>
<td>$$$$</td>
<td>$$</td>
</tr>
<tr>
<td>Assembly cost</td>
<td>$$$</td>
<td>$$$$$</td>
<td>$</td>
</tr>
</tbody>
</table>

CONFIDENTIAL INFORMATION
Thermally engineered material (Met-Graf) developed start-up MMCC – acquired 2015 by Parker Hannifin

PCB fabrication technology developed and patented by Lockheed Martin under US Patent No. 8,245,390 B2 issued on 21 August 2012

Cirexx involved in process and technology development through PCB manufacturing. First PCBs fabricated and tested in 2009.

Cirexx licensed by LMCO M&FC in 2013. The technology is currently used on production programs

Demonstration Reference System, White Paper and presentation available
Multilayered PCB Structure with 2 Composite Cores and a Die-Attached MMIC
APPLICATIONS

Technology Introduction

High Power RF (millimeter wave)
Phased Array Radar
Missile Guidance
Satellites & Space systems

Product Maturity

Super Computing/CPU
”Down Hole” Sensors & Controls
Electronic sub-systems (mezzanine)

Mass Production

Automotive/Sensors and Controls
Consumer & Industrial LED & CCD
Consumer Communications
Thermally engineered material is a graphite copper composite which acts essentially as a “metal-core”. Available in 10, 20 and 40 mil thickness.

Vacuum processing assures no residual organics for outgassing or corrosion

Superior thermal conductivity competing with best currently available materials for PCBs

Ceramic-matched CTE (especially Z axis) allows for direct-attach of GaAs & GaN die to PCB

Thinner and lighter-weight heat sinking vs. aluminum or copper metal-core (6 g/cm³)

CTE and “balanced stack up” reduces probability of PCB warping and twisting
## TECHNICAL DATA

<table>
<thead>
<tr>
<th>Feature</th>
<th>Unit</th>
<th>Epoxy</th>
<th>Graphite Epoxy</th>
<th>OFHC Copper</th>
<th>Aluminum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Conductivity</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>x - y axis W/mK</td>
<td>285 - 300</td>
<td>0.5</td>
<td>175</td>
<td>390</td>
<td>160</td>
</tr>
<tr>
<td>Z axis W/mK</td>
<td>210</td>
<td>0.5</td>
<td>1</td>
<td>390</td>
<td>160</td>
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<tr>
<td>Heat Capacity (Cp)</td>
<td>J/g-K</td>
<td>0.433</td>
<td>0.6</td>
<td></td>
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<tr>
<td>CTE (avg 20°C to 150°C)</td>
<td>ppm/C</td>
<td>7</td>
<td>55</td>
<td>6.5</td>
<td>17</td>
</tr>
<tr>
<td>x - y axis ppm/C</td>
<td>7</td>
<td>55</td>
<td>6.5</td>
<td>17</td>
<td>25</td>
</tr>
<tr>
<td>Z axis ppm/C</td>
<td>16</td>
<td>55</td>
<td>55</td>
<td>17</td>
<td>25</td>
</tr>
<tr>
<td>Tensile Strength</td>
<td>ksi</td>
<td>10</td>
<td></td>
<td>34 - 46</td>
<td>40.0</td>
</tr>
<tr>
<td>x - y axis</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Z axis</td>
<td>5</td>
<td></td>
<td></td>
<td>34 - 46</td>
<td>40.0</td>
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<tr>
<td>Compressive Strength</td>
<td>ksi</td>
<td>28.5</td>
<td></td>
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<tr>
<td>Yield Strength (composite)</td>
<td>ksi</td>
<td>12.2</td>
<td></td>
<td>26 - 44</td>
<td>45.0</td>
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<tr>
<td>Elastic Modulus (Young's)</td>
<td>msi</td>
<td>11</td>
<td>3.5</td>
<td>11</td>
<td>17</td>
</tr>
<tr>
<td>Resistivity</td>
<td>μΩcm</td>
<td>4.36</td>
<td>2.85</td>
<td>1.71</td>
<td>0.04</td>
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<tr>
<td>Density</td>
<td>g/cc</td>
<td>6.07</td>
<td>1.65</td>
<td>9.10</td>
<td>2.70</td>
</tr>
<tr>
<td>Machinability (drill/rout)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Plated Metal Adhesion</td>
<td>excellent</td>
<td></td>
<td>fair</td>
<td>good</td>
<td>good</td>
</tr>
<tr>
<td>Lamination Adhesives</td>
<td>standard</td>
<td></td>
<td>fair</td>
<td>excellent</td>
<td>good</td>
</tr>
</tbody>
</table>
PCB Constructions available with many common materials: polyimides, PTFEs, and ceramic-filled laminates

“Cap Construction” with Arlon 85NT, or “Foil Construction with Taconic TPG30 are common

Processing similar to standard PCB methods and equipment

ENEPIG (electroless nickel, electroless palladium, immersion gold) best finish for wire bonding

Composite backfilled – when required - with low CTE material

End product complies with IPC-6013, 6018 and MIL-PRF-31032
A typical PCB construction with advanced RF dielectrics and RF pre-pregs and direct die-attach.
**PCB Construction**

- "P" (pitch between closest similar via)
- "D" (drilled hole diameter)

**Typical Signal Via**
- Top Layer Signals
- Outer Core
- Pre-Preg
- Met-Graf/Ground
- Pre-Preg
- Inner layer Signals
- Inner Core
- Inner layer Signals
- Pre-Preg
- Inner layer Signals
- Inner Core
- Inner layer Signals
- Pre-Preg
- Met-Graf/Ground
- Pre-Preg
- Outer Core
- Bottom Layer Signals

**Typical Thermal Via**
- Through hole plating directly against Met-Graf for electrical contact
- Pre-Preg flow into pre-drilled hole in sequential lam set for electrical isolation
- Pre-drilled hole in Met-Graf filled for electrical isolation
- Via pad

**Confidential Information**

- Smallest standard drill hole diameter is 10:1 ratio between D:T (drilled hole diameter to overall board thickness)
- Smallest standard Via pad is D + 25 mils (drill diameter plus 0.025")
- Smallest standard Signal Via pitch is D + 30 mils (drill diameter plus 0.030")
- Smallest standard Thermal Via pitch is D + 15 mils (drill diameter plus 0.015")
- Minimum Met-Graf clearance hole drill is D + 35 mils (drilled hole diameter plus 0.035")
- Minimum Thermal Via clearance hole drill (though sequential lam set) is D + 30 mils (drilled hole diameter plus 0.030")
Cross-section of typical thermal via through ECLIPS PCB

- Pad on Top Layers
- Pad on Bottom Layer
- Internal Ground Connections
- Engineering metalized material layers
Cross-section of typical signal via through ECLIPS PCB

- Pad on Top Layers
- Internal metalized layer pre-drilled and backfilled
- Internal Signal Connection
- (Bottom Layer not shown)
Cross-section of typical laser cavity through ECLIPS PCB

- Laser Ablated Cavity
- Top Layer
- Engineering metalized material layer

(Remainder of board not shown)
After Copper Plating Process

After Thermal Stress Test
Signal Via Spacing

Center-Core Construction

Micro Vias

Thermal Via Spacing
Cross-section of typical ECLIPS PCB after Laser Cavity Ablating Operation

- Laser ablated cavity through outer core & pre-preg to expose Met-Graf (±.001")
- Die placed in cavity and attached with epoxy or solder
- Nickel/Gold plating in cavity bottom over Met-Graf

Cross-section of typical ECLIPS PCB with MMIC die-attached

- Wire Bonding (.25 to 1 mil ribbons)
- Met-Graf Copper/Graphite Composite Layer
- Pre-Preg
- Inner Core
- Outer Core
“Chip & Wire” die attached into outer core cavity directly onto composite layer with solder (AuSn) or silver epoxy paste eliminated the need for exotic heat sinking

1 mil Au wire bonding for DC; .25 mil wire for RF connectivity

Standard SMT assembly of “plastic parts” for remainder of PCB - vapor phase soldering

Low CTE assures component survival and reliability at higher temperatures

Housing can be easily machined from anodized aluminum
Wire/ribbon bonding of direct die-attach to PCB
Exploded view of high power amplifier with ECLIPS PCB – GaN die side up

Aluminum milled chassis is electrical and thermal common ground

Exploded view of high power amplifier with ECLIPS PCB – GaN die side down
ECLIPS Technology provides a lower cost, more reliable alternative to Co-Fired Ceramic or Hybrid MIC when needing to use both direct die-attach and SMT components.

Alternatives unreliable and expensive:
- Ceramics are very high cost
- Hybrid MIC (w/glass feed-through) are labor intensive and much larger

Cirexx engineers are prepared and able to convert your existing designs to an ECLIPS Technology or help you to develop a new one.

ECLIPS Technology meets all current standards and specification.